

Application No. : 09/808,469
Filed : March 14, 2001

APPENDIX-XH

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Instruction formats

i = instruction opcode
 a = register (r0-3,r13-16)
 b = register (r0-3,r13-16)
 5 e = register (r0-3,r13-16)
 h = register high (r0-r31)
 q = condition code
 u = unsigned immediate
 s = signed immediate

Op	Format	Instruction	Operands	Comment	
0	iiiiqqssssssss	bal/beq/bne	s8	; if cc pc=(pc&0xffffffff)+(s8<<1)	
	iiii1lqqssssss	bgt/bge/blt/ble	s6	; if cc pc=(pc&0xffffffff)+(s6<<1)	
1	iiiiisssssssss	bl	s10	; blink=pc, pc=(pc&0xffffffff)+(s10<<2)	
2	iiiiaaabbibi	op	a,a,b	; op = sub/and/or/xor/asl/asr/lsl/l	
			a,b,1	asl1/asrl/	
			a,b,2	asl2/asr2/	
			0,a,b	and.f/mul64/?/?/s_op	
20	iiiiaaaaii1lll	s_op	a,a	; s_op=extb/extw/sexb/sextw/	
			[a]	j/j1/	
			a,a,a	sub.ne/i_op	
	iiiiiiii1111111	i_op3		; i_op=brk/j [blink]/st blink[sp,4]/	
3	iiiiaaaaiuuuuuu	mov/cmp	a,u6		
4	iiiiaaaaiiuuuuu	add/sub/?/?	a,a,u5		
25	5	iiiiaaaahhh00hh	mov	a,h	
	iiiiaaaahhh01hh	add	a,a,h		
	iiiiaaaahhh1hhh	mov/cmp	h,a		
6	iiiiaaaa000iuuu	ld/st	a,[fp,-u3]	; a=mem[fp-(u3 << 2)]	
	iiiiaaaa001iuuu	add/?	a,[fp,-u3]	; a=fp-(u3 << 2)	
30	iiiiaaaaiiuuuuu	asl/asr/lsl	a,a,u5		
	7	iiiiaaabbuuuu	ld	a,[b,u4]	; a=mem[b+(u4<<2)]
	8	iiiiaaabbuuuu	ldb	a,[b,u4]	; a=mem[b+u4]
	9	iiiiaaabbuuuu	ldw	a,[b,u4]	; a=mem[b+(u4<<1)]
A	iiiiaaabbuuuu	st	a,[b,u4]	; a=mem[b+(u4<<2)]	
B	iiiiaaabb0uuu	stb	a,[b,u3]	; a=mem[b+u3]	
C	iiiiaaabb1uuu	stw	a,[b,u3]	; a=mem[b+(u3<<1)]	
D	iiiiaaauiuuuuuu	add/sub	a,b,u3	; a=b op u3	
E	iiiiaaauiuuuuuu	ld	a,[pc,u7]	; a=mem[(pc&0xffffffff)+(u7 << 2)]	
F	iiii*****	reserved	a,[gp,u7]	; a=mem[gp+(u7 << 2)]	
	<u>Other possible formats:</u>				
	iiiiaaabb0eee	ld	a,[b,e]	; a=mem[b+e]	
	iiiiaaabb1eee	add	a,b,c	; a=b+c	
45	iiiiaaauiuuuuuu	add	a,pc,u7	; a=(pc&0xffffffff)+(u7 << 2)	